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A cross-sectional view of a GaN-based semiconductor device structure. The structure is built on an n-SiC Substrate (23). Above the substrate is an n-AlGaIn buffer layer (10). This is followed by a stack of alternating layers: n-GaN (12), n-GaN (14), and a multi-layered region (16) consisting of alternating thin layers of InGaIn and GaN. Above this stack is a p-type region (17) consisting of alternating layers of GaN, InGaIn, and p-AlGaIn. The topmost layer is p-GaN (24). Various reference numerals point to specific layers and regions: 100 points to the top surface, 118 points to the p-type region, 125 points to the n-type region, 120 points to the interface between the p-type and n-type regions, 12 points to the n-GaN layer, 14 points to the n-GaN layer, 11 points to the n-AlGaIn buffer, 10 points to the n-AlGaIn buffer, 23 points to the n-SiC Substrate, 24 points to the p-GaN layer, 32 points to the p-AlGaIn layer, 30 points to the AlGaIn layer, and 22 points to the GaN layer.

**(57) Abstract:** A light emitting diode is provided having a Group III nitride based superlattice and a Group III nitride based active region on the superlattice. The active region has at least one quantum well structure. The quantum well structure includes a first Group III nitride based barrier layer, a Group III nitride based quantum well layer on the first barrier layer and a second Group III nitride based barrier layer. A Group III nitride based semiconductor device and methods of fabricating a Group III nitride based semiconductor device having an active region comprising at least one quantum well structure are provided. The quantum well structure includes a well support layer comprising a Group III nitride, a quantum well layer comprising a Group III nitride on the well support layer and a cap layer comprising a Group III nitride on the quantum well layer. A Group III nitride based semiconductor device is also provided that includes a gallium nitride based superlattice having at least two periods of alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$ , where  $0 \leq X < 1$  and  $0 \leq Y < 1$  and  $X$  is not equal to  $Y$ . The semiconductor device may be a light emitting diode with a Group III nitride based active region. The active region may be a multiple quantum well active region.

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LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

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Internal application No  
PCT/US 02/16407

**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>US 6 153 894 A (SHOWA DENKO CO) 28 November 2000 (2000-11-28)</p> <p>column 7, line 21 -column 10, line 33 column 11, line 51 -column 15, line 39; claims 1-4; example 1 --- -/-</p>	<p>1,3,5-8, 10-13, 15, 17-20, 22-33, 36-38, 41-44, 47, 49-55, 58-61, 63,64, 66-79</p>

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>PATENT ABSTRACTS OF JAPAN vol. 1999, no. 05, 31 May 1999 (1999-05-31) &amp; JP 11 040850 A (TOYODA GOSEI CO), 12 February 1999 (1999-02-12)</p> <p>paragraphs '0014!-'0022!</p>	<p>1,3,5-7, 10-13, 15,17, 18, 22-25, 27-33, 35-37, 40-43, 47, 49-54, 58-60, 62-64, 66-75, 77,79,93</p>
X	<p>WO 00 76004 A (NICHIA CORP) 14 December 2000 (2000-12-14)</p> <p>-&amp; EP 1 189 289 A (NICHIA CORP) 20 March 2002 (2002-03-20) paragraphs '0004!-'0018!; examples 1,9-13</p>	<p>1,3,5-7, 10,12, 13,15, 17-20, 22-25, 27-37, 40-43, 47, 49-55, 58,59, 62-64, 66-79</p>
A	<p>WO 00 21143 A (OSRAM OPTO SEMICONDUCTORS) 13 April 2000 (2000-04-13) the whole document</p>	<p>1,10,11, 33,40,41</p>
P,X	<p>WO 02 05399 A (NICHIA CORP) 17 January 2002 (2002-01-17) -&amp; US 2002/053676 A1 (NICHIA CORP) 9 May 2002 (2002-05-09) examples 1,13,14</p>	<p>1-105</p>

**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-57,79-105

Group III nitride based semiconductor device comprising a quantum well structure

2. Claims: 1-32,58-78

Group III nitride based semiconductor device comprising a superlattice structure

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US 02/16407

## Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:  
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. ☐ Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

## Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

## INTERNATIONAL SEARCH REPORT

information on patent family members

Internal

Application No

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Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6153894	A	28-11-2000	JP 2000150957 A DE 19954242 A1 TW 432725 B	30-05-2000 25-05-2000 01-05-2001
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(54) Title: GROUP III NITRIDE BASED LIGHT EMITTING DIODE STRUCTURES WITH A QUANTUM WELL AND SUPERLATTICE, GROUP III NITRIDE BASED QUANTUM WELL STRUCTURES AND GROUP III NITRIDE BASED SUPERLATTICE STRUCTURES

(57) Abstract: A light emitting diode is provided having a Group III nitride based superlattice and a Group III nitride based active region on the superlattice. The active region has at least one quantum well structure. The quantum well structure includes a first Group III nitride based barrier layer, a Group III nitride based quantum well layer on the first barrier layer and a second Group III nitride based barrier layer. A Group III nitride based semiconductor device and methods of fabricating a Group III nitride based semiconductor device having an active region comprising at least one quantum well structure are provided. The quantum well structure includes a well support layer comprising a Group III nitride, a quantum well layer comprising a Group III nitride on the well support layer and a cap layer comprising a Group III nitride on the quantum well layer. A Group III nitride based semiconductor device is also provided that includes a gallium nitride based superlattice having at least two periods of alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$ , where  $0 \leq x < 1$  and  $0 \leq y < 1$  and  $x$  is not equal to  $y$ . The semiconductor device may be a light emitting diode with a Group III nitride based active region. The active region may be a multiple quantum well active region.

WO 02/097904 A2



**GROUP III NITRIDE BASED LIGHT EMITTING DIODE STRUCTURES  
WITH A QUANTUM WELL AND SUPERLATTICE, GROUP III NITRIDE  
BASED QUANTUM WELL STRUCTURES AND GROUP III NITRIDE  
BASED SUPERLATTICE STRUCTURES**

**Cross-Reference to Provisional Application**

This application claims the benefit of, and priority from, Provisional  
Application Serial No. 60/294,445, filed May 30, 2001 entitled *MULTI-QUANTUM  
WELL LIGHT EMITTING DIODE STRUCTURE*, Provisional Application Serial No.  
5 60/294,308, filed May 30, 2001 entitled *LIGHT EMITTING DIODE STRUCTURE  
WITH SUPERLATTICE STRUCTURE* and Provisional Application Serial No.  
60/294,378, filed May 30, 2001 entitled *LIGHT EMITTING DIODE STRUCTURE  
WITH MULTI-QUANTUM WELL AND SUPERLATTICE STRUCTURE*, the  
disclosures of which are hereby incorporated herein by reference in their entirety as if  
10 set forth fully herein.

**Field of the Invention**

This invention relates to microelectronic devices and fabrication methods  
therefor, and more particularly to structures which may be utilized in Group III nitride  
15 semiconductor devices, such as light emitting diodes (LEDs).

**Background of the Invention**

Light emitting diodes are widely used in consumer and commercial  
applications. As is well known to those having skill in the art, a light emitting diode  
20 generally includes a diode region on a microelectronic substrate. The microelectronic  
substrate may comprise, for example, gallium arsenide, gallium phosphide, alloys  
thereof, silicon carbide and/or sapphire. Continued developments in LEDs have  
resulted in highly efficient and mechanically robust light sources that can cover the  
visible spectrum and beyond. These attributes, coupled with the potentially long

service life of solid state devices, may enable a variety of new display applications, and may place LEDs in a position to compete with the well entrenched incandescent lamp.

One difficulty in fabricating Group III nitride based LEDs, such as gallium nitride based LEDs, has been with the fabrication of high quality gallium nitride. Typically, gallium nitride LEDs have been fabricated on sapphire or silicon carbide substrates. Such substrates may result in mismatches between the crystal lattice of the substrate and the gallium nitride. Various techniques have been employed to overcome potential problems with the growth of gallium nitride on sapphire and/or silicon carbide. For example, aluminum nitride (AlN) may be utilized as a buffer between a silicon carbide substrate and a Group III active layer, particularly a gallium nitride active layer. Typically, however, aluminum nitride is insulating rather than conductive. Thus, structures with aluminum nitride buffer layers typically require shorting contacts that bypass the aluminum nitride buffer to electrically link the conductive silicon carbide substrate to the Group III nitride active layer.

Alternatively, conductive buffer layer materials such as gallium nitride (GaN), aluminum gallium nitride (AlGaIn), or combinations of gallium nitride and aluminum gallium nitride may allow for elimination of the shorting contacts typically utilized with AlN buffer layers. Typically, eliminating the shorting contact reduces the epitaxial layer thickness, decreases the number of fabrication steps required to produce devices, reduces the overall chip size, and/or increases the device efficiency. Accordingly, Group III nitride devices may be produced at lower cost with a higher performance. Nevertheless, although these conductive buffer materials offer these advantages, their crystal lattice match with silicon carbide is less satisfactory than is that of aluminum nitride.

The above described difficulties in providing high quality gallium nitride may result in reduced efficiency the device. Attempts to improve the output of Group III nitride based devices have included differing configurations of the active regions of the devices. Such attempts have, for example, included the use of single and/or double heterostructure active regions. Similarly, quantum well devices with one or more Group III nitride quantum wells have also been described. While such attempts have improved the efficiency of Group III based devices, further improvements may still be achieved.

### Summary of the Invention

Embodiments of the present invention provide a light emitting diode having a Group III nitride based superlattice and a Group III nitride based active region on the superlattice. The active region has at least one quantum well structure. The quantum well structure includes a first Group III nitride based barrier layer, a Group III nitride based quantum well layer on the first barrier layer and a second Group III nitride based barrier layer on the quantum well layer.

In further embodiments of the present invention, the light emitting diode includes from about 2 to about 10 repetitions of the at least one quantum well structure.

In additional embodiments of the present invention, the superlattice includes a gallium nitride based superlattice having at least two periods of alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$ , where  $0 \leq X < 1$  and  $0 \leq Y < 1$  and  $X$  is not equal to  $Y$ . The first Group III nitride based barrier layer provides a well support layer comprising a Group III nitride and the second Group III nitride based barrier layer provides a cap layer comprising a Group III nitride on the quantum well layer.

In such embodiments, the cap layer may have a lower crystal quality than the well support layer.

In still further embodiments of the present invention, the well support layer comprises a gallium nitride based layer, the quantum well layer comprises an indium gallium nitride layer and the barrier layer comprises a gallium nitride based layer. In such embodiments, the well support layer and the cap layer may be provided by layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  where  $0 \leq X < 1$ . Furthermore, the indium composition of the well support layer and the cap layer may be less than the indium composition of the quantum well layer.

The well support layer and the cap layer may also be provided by a layer of  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$  where  $0 < X < 1$ ,  $0 \leq Y < 1$  and  $X + Y \leq 1$ . Furthermore, the well support layer and the cap layer may be undoped. Alternatively, the well support layer and the cap layer may have an n-type doping level of less than about  $5 \times 10^{19} \text{ cm}^{-3}$ . The cap layer and the well support layer may also have a higher bandgap than the quantum well layer. The combined thickness of the well support layer and the cap layer may be from about 50 to about 400 Å. The thickness of the well support layer may be greater than a thickness of the cap layer. The quantum well layer may have a

thickness of from about 10 to about 50 Å. For example, the quantum well layer may have a thickness of about 20 Å. Furthermore, the percentage of indium in the quantum well layer may be from about 15% to about 40%.

In additional embodiments of the present invention, a Group III nitride based spacer layer is provided between the well support layer and the superlattice. The  
5 spacer layer may be undoped GaN.

In other embodiments of the present invention, the bandgap of the quantum well is less than the bandgap of the superlattice.

In further embodiments of the present invention, the light emitting diode  
10 includes a second well support layer comprising a Group III nitride on the cap layer, a second quantum well layer comprising a Group III nitride on the second well support layer and a second cap layer comprising a Group III nitride on the second quantum well layer.

In additional embodiments of the present invention, the gallium nitride based  
15 superlattice comprises from about 5 to about 50 periods. The alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  may have a combined thickness of from about 10 to about 140 Å.

In particular embodiments of the present invention,  $X = 0$  for layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  of the superlattice. In such embodiments, the InGaN layers may have a thickness  
20 of from about 5 to about 40 Å and the GaN layers may have a thickness of from about 5 to about 100 Å.

In further embodiments of the present invention, the gallium nitride based superlattice is doped with an n-type impurity to a level of from about  $1 \times 10^{17} \text{ cm}^{-3}$  to about  $5 \times 10^{19} \text{ cm}^{-3}$ . The doping level of the gallium nitride based superlattice may be  
25 an actual doping level of layers of the alternating layers. The doping level may also be an average doping level of layers of the alternating layers. Thus, for example, the light emitting diode may include doped Group III nitride layers adjacent the superlattice where the doped Group III nitride layers are doped with an n-type impurity to provide an average doping of the doped Group III nitride layers and the  
30 superlattice of from about  $1 \times 10^{17} \text{ cm}^{-3}$  to about  $5 \times 10^{19} \text{ cm}^{-3}$ . The bandgap of the superlattice may be from about 2.95 eV to about 3.35 eV and, in certain embodiments, may be about 3.15 eV.

In other embodiments of the present invention, a Group III nitride based semiconductor device having an active region comprising at least one quantum well

structure is provided. The quantum well structure includes a well support layer comprising a Group III nitride, a quantum well layer comprising a Group III nitride on the well support layer and a cap layer comprising a Group III nitride on the quantum well layer.

- 5           The cap layer may have a lower crystal quality than the well support layer. The well support layer may be provided by a gallium nitride based layer, the quantum well layer may be provided by an indium gallium nitride layer and the barrier layer may be provided by a gallium nitride based layer. In such embodiments, the well support layer and the cap layer may be provided by layers of  $\text{In}_X\text{Ga}_{1-X}\text{N}$  where
- 10    $0 \leq X < 1$ . Furthermore, the indium composition of the well support layer and the cap layer may be less the indium composition of the quantum well layer. Similarly, the well support layer and the cap layer may be provided by layers of  $\text{Al}_X\text{In}_Y\text{Ga}_{1-X-Y}\text{N}$  where  $0 < X < 1$ ,  $0 \leq Y < 1$  and  $X + Y \leq 1$ .

Furthermore, the well support layer and the cap layer may be undoped.

- 15   Alternatively, the well support layer and the cap layer may have a doping level of less than about  $5 \times 10^{19} \text{ cm}^{-3}$ .

- In further embodiments of the present invention, the cap layer and the well support layer have a higher bandgap than the quantum well layer. The combined thickness of the well support layer and the cap layer may be from about 50 to about
- 20   400 Å. For example, the combined thickness of the well support layer and the cap layer may be greater than about 90 Å. Similarly, the combined thickness of the well support layer and the cap layer may be about 225 Å. The thickness of the well support layer may be greater than the thickness of the cap layer.

- In additional embodiments of the present invention, the quantum well layer
- 25   has a thickness of from about 10 to about 50 Å. For example, the quantum well layer may have a thickness of about 25 Å. Furthermore, the percentage of indium in the quantum well layer may from about 5% to about 50%.

- In further embodiments of the Group III nitride based semiconductor device
- 30   according to the present invention, a superlattice is provided and the well support layer is on the superlattice. The superlattice may have a bandgap of about 3.15 eV. Furthermore, a Group III nitride based spacer layer may be provided between the well support layer and the superlattice. The spacer layer may be undoped GaN. Also, the

bandgap of the at least one quantum well may be less than the bandgap of the superlattice.

In still further embodiments of the present invention, a second well support layer comprising a Group III nitride is provided on the cap layer. A second quantum well layer comprising a Group III nitride is provided on the second well support layer; and a second cap layer comprising a Group III nitride is provided on the second quantum well layer.

In particular embodiments of the present invention, the Group III nitride based semiconductor device includes from about 2 to about 10 repetitions of the at least one quantum well structures.

Embodiments of the present invention further provide a Group III nitride based semiconductor device that includes a gallium nitride based superlattice having at least two periods of alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$ , where  $0 \leq X < 1$  and  $0 \leq Y < 1$  and  $X$  is not equal to  $Y$ .

In further embodiments of the present invention, the gallium nitride based superlattice includes from about 5 to about 50 periods. For example, the gallium nitride based superlattice may include 25 periods. Similarly, the gallium nitride based superlattice may include 10 periods.

In additional embodiments of the present invention, the gallium nitride based superlattice comprises from about 5 to about 50 periods. The alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  may have a combined thickness of from about 10 to about 140 Å.

In particular embodiments of the present invention,  $X = 0$  for layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  of the superlattice. In such embodiments, the InGaN layers may have a thickness of from about 5 to about 40 Å and the GaN layers may have a thickness of from about 5 to about 100 Å. In still further embodiments of the present invention, the gallium nitride based superlattice is doped with an n-type impurity to a level of from about  $1 \times 10^{17} \text{ cm}^{-3}$  to about  $5 \times 10^{19} \text{ cm}^{-3}$ . The doping level of the gallium nitride based superlattice may be an actual doping level of layers of the alternating layers or may be an average doping level of layers of the alternating layers.

In certain embodiments of the present invention, doped Group III nitride layers are provided adjacent the superlattice. The doped Group III nitride layers are doped with an n-type impurity to provide an average doping of the doped Group III nitride layers and the superlattice of from about  $1 \times 10^{17} \text{ cm}^{-3}$  to about  $5 \times 10^{19} \text{ cm}^{-3}$ .

In additional embodiments of the present invention, a bandgap of the superlattice is about 3.15 eV.

In embodiments of the present invention where the Group III nitride based semiconductor device comprises a light emitting diode, the light emitting diode  
5 includes a Group III nitride based active region on the superlattice. Additionally, a Group III nitride based spacer layer may also be provided between the active region and the superlattice. Such a spacer layer may be undoped GaN.

In certain embodiments of the present invention, the active region comprises at least one quantum well. In such embodiments, a bandgap of the quantum well may be  
10 less than a bandgap of the superlattice.

Additional embodiments of the present invention provide a method of fabricating a Group III nitride based semiconductor device having an active region comprising at least one quantum well structure. The quantum well structure is fabricated by forming a well support layer comprising a Group III nitride, forming a  
15 quantum well layer comprising a Group III nitride on the quantum well support layer and forming a cap layer comprising a Group III nitride on the quantum well layer.

In particular embodiments of the present invention, forming a well support layer comprising a Group III nitride is provided by forming the well support layer at a first temperature. Forming a quantum well layer is provided by forming the quantum  
20 well layer at a second temperature which is less than the first temperature. Forming a cap layer is provided by forming the cap layer at a third temperature which is less than the first temperature. In certain embodiments of the present invention, the third temperature is substantially the same as the second temperature.

In further embodiments of the present invention, the well support layer  
25 comprises a gallium nitride based layer, the quantum well layer comprises an indium gallium nitride layer and the cap layer comprises a gallium nitride based layer. In such embodiments, the first temperature may be from about 700 to about 900 °C. Furthermore, the second temperature may be from about 0 to about 200 °C less than the first temperature. The indium gallium nitride layer may be formed in a nitrogen  
30 atmosphere or other atmosphere.

Preferably, forming a well support layer and forming a cap layer are provided by forming a cap layer of  $\text{In}_x\text{Ga}_{1-x}\text{N}$ , where  $0 \leq x < 1$  and forming a well support layer

of  $\text{In}_x\text{Ga}_{1-x}\text{N}$ , where  $0 \leq x < 1$ . Also, the indium composition of the well support layer and the cap layer may be less an indium composition of the quantum well layer.

In additional embodiments of the present invention, forming a well support layer and forming a cap layer are provided by forming a cap layer of  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ ,  
5 where  $0 < x < 1$ ,  $0 \leq y < 1$  and  $x + y \leq 1$  and forming a well support layer of  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ , where  $0 < x < 1$ ,  $0 \leq y < 1$  and  $x + y \leq 1$ .

Further embodiments of the present invention include forming a superlattice, where the well support layer is on the superlattice. Additional embodiments of the present invention include, forming a Group III nitride based spacer layer between the  
10 well support layer and the superlattice. The spacer layer may be undoped GaN. Additional embodiments of the present invention include forming a second well support layer comprising a Group III nitride on the cap layer, forming a second quantum well layer comprising a Group III nitride on the second well support layer and forming a second cap layer comprising a Group III nitride on the second quantum  
15 well layer. In such embodiments, the second well support layer may be formed at substantially the first temperature, the second quantum well layer may be formed at substantially the second temperature which is less than the first temperature and the second cap layer formed at substantially the third temperature which is less than the first temperature.

20

### **Brief Description of the Drawings**

Other features of the present invention will be more readily understood from the following detailed description of specific embodiments thereof when read in  
25 conjunction with the accompanying drawings, in which:

**Figure 1** is a schematic illustration of a Group III nitride light emitting diode incorporating embodiments of the present invention;

**Figure 2** is a schematic illustration of a Group III nitride light emitting diode incorporating further embodiments of the present invention; and

30 **Figure 3** is a schematic illustration of a quantum well structure and a multi-quantum well structure according to additional embodiments of the present invention.



### Detailed Description of Preferred Embodiments

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

Embodiments of the present invention will be described with reference to **Figure 1** that illustrates a light emitting diode (LED) structure **40**. The LED structure **40** of **Figure 1** includes a substrate **10**, which is preferably 4H or 6H n-type silicon carbide. Substrate **10** may also comprise sapphire, bulk gallium nitride or another suitable substrate. Also included in the LED structure **40** of **Figure 1** is a layered semiconductor structure comprising gallium nitride-based semiconductor layers on substrate **10**. Namely, the LED structure **40** illustrated includes the following layers: a conductive buffer layer **11**, a first silicon-doped GaN layer **12**, a second silicon doped GaN layer **14**, a superlattice structure **16** comprising alternating layers of silicon-doped GaN and/or InGaN, an active region **18**, which may be provided by a multi-quantum well structure, an undoped GaN and/or AlGaN layer **22**, an AlGaN layer **30** doped with a p-type impurity, and a GaN contact layer **32**, also doped with a p-type impurity. The structure further includes an n-type ohmic contact **23** on the substrate **10** and a p-type ohmic contact **24** on the contact layer **32**.

Buffer layer **11** is preferably n-type AlGaN. Examples of buffer layers between silicon carbide and group III-nitride materials are provided in U.S. Patents 5,393,993 and 5,523,589, and U.S. Application Serial No. 09/154,363 entitled "Vertical Geometry InGaN Light Emitting Diode" assigned to the assignee of the present invention, the disclosures of which are incorporated by reference as if fully set

forth herein. Similarly, embodiments of the present invention may also include structures such as those described in United States Patent No. 6,201,262 entitled "Group III Nitride Photonic Devices on Silicon Carbide Substrates With Conductive Buffer Interlay Structure," the disclosure of which is incorporated herein by reference  
5 as if set forth fully herein.

GaN layer 12 is preferably between about 500 and 4000 nm thick inclusive and is most preferably about 1500 nm thick. GaN layer 12 may be doped with silicon at a level of about  $5 \times 10^{17}$  to  $5 \times 10^{18} \text{ cm}^{-3}$ . GaN layer 14 is preferably between about 10 and 500 Å thick inclusive, and is most preferably about 80 Å thick. GaN layer 14  
10 may be doped with silicon at a level of less than about  $5 \times 10^{19} \text{ cm}^{-3}$ .

As illustrated in Figure 1, a superlattice structure 16 according to embodiments of the present invention includes alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$ , wherein X is between 0 and 1 inclusive and X is not equal to Y. Preferably,  $X=0$  and the thickness of each of the alternating layers of InGaN is about  
15 5-40 Å thick inclusive, and the thickness of each of the alternating layers of GaN is about 5-100 Å thick inclusive. In certain embodiments, the GaN layers are about 30 Å thick and the InGaN layers are about 15 Å thick. The superlattice structure 16 may include from about 5 to about 50 periods (where one period equals one repetition each of the  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  layers that comprise the superlattice). In one  
20 embodiment, the superlattice structure 16 comprises 25 periods. In another embodiment, the superlattice structure 16 comprises 10 periods. The number of periods, however, may be decreased by, for example, increasing the thickness of the respective layers. Thus, for example, doubling the thickness of the layers may be utilized with half the number of periods. Alternatively, the number and thickness of  
25 the periods may be independent of one another.

Preferably, the superlattice 16 is doped with an n-type impurity such as silicon at a level of from about  $1 \times 10^{17} \text{ cm}^{-3}$  to about  $5 \times 10^{19} \text{ cm}^{-3}$ . Such a doping level may be actual doping or average doping of the layers of the superlattice 16. If such doping level is an average doping level, then it may be beneficial to provide doped layers  
30 adjacent the superlattice structure 16 that provide the desired average doping which the doping of the adjacent layers is averaged over the adjacent layers and the superlattice structure 16. By providing the superlattice 16 between substrate 10 and active region 18, a better surface may be provided on which to grow InGaN-based active region 18. While not wishing to be bound by any theory of operation, the

inventors believe that strain effects in the superlattice structure 16 provide a growth surface that is conducive to the growth of a high-quality InGaN-containing active region. Further, the superlattice is known to influence the operating voltage of the device. Appropriate choice of superlattice thickness and composition parameters can  
5 reduce operating voltage and increase optical efficiency.

The superlattice structure 16 may be grown in an atmosphere of nitrogen or other gas, which enables growth of higher-quality InGaN layers in the structure. By growing a silicon-doped InGaN/GaN superlattice on a silicon-doped GaN layer in a nitrogen atmosphere, a structure having improved crystallinity and conductivity with  
10 optimized strain may be realized.

In certain embodiments of the present invention, the active region 18 may comprise a single or multi-quantum well structure as well as single or double heterojunction active regions. In particular embodiments of the present invention, the active region 18 comprises a multi-quantum well structure that includes multiple  
15 InGaN quantum well layers separated by barrier layers (not shown in Figure 1).

Layer 22 is provided on active region 18 and is preferably undoped GaN or AlGaIn between about 0 and 120 Å thick inclusive. As used herein, undoped refers to a not intentionally doped. Layer 22 is preferably about 35 Å thick. If layer 22 comprises AlGaIn, the aluminum percentage in such layer is preferably about 10-30%  
20 and most preferably about 24%. The level of aluminum in layer 22 may also be graded in a stepwise or continuously decreasing fashion. Layer 22 may be grown at a higher temperature than the growth temperatures in quantum well region 25 in order to improve the crystal quality of layer 22. Additional layers of undoped GaN or AlGaIn may be included in the vicinity of layer 22. For example, LED 1 may include  
25 an additional layer of undoped AlGaIn about 6-9 Å thick between the active region 18 and the layer 22.

An AlGaIn layer 30 doped with a p-type impurity such as magnesium is provided on layer 22. The AlGaIn layer 30 may be between about 0 and 300 Å thick inclusive and is preferably about 130 Å thick. A contact layer 32 of p-type GaN is  
30 provided on the layer 30 and is preferably about 1800 Å thick. Ohmic contacts 24 and 25 are provided on the p-GaN contact layer 32 and the substrate 10, respectively.

Figure 2 illustrates further embodiments of the present invention incorporating a multi-quantum well active region. The embodiments of the present invention illustrated in Figure 2 include a layered semiconductor structure 100

comprising gallium nitride-based semiconductor layers grown on a substrate 10. As described above, the substrate 10 may be SiC, sapphire or bulk gallium nitride. As is illustrated in Figure 2, LEDs according to particular embodiments of the present invention may include a conductive buffer layer 11, a first silicon-doped GaN layer 12, a second silicon doped GaN layer 14, a superlattice structure 16 comprising alternating layers of silicon-doped GaN and/or InGaN, an active region 125 comprising a multi-quantum well structure, an undoped GaN or AlGaN layer 22, an AlGaN layer 30 doped with a p-type impurity, and a GaN contact layer 32, also doped with a p-type impurity. The LEDs may further include an n-type ohmic contact 23 on the substrate 10 and a p-type ohmic contact 24 on the contact layer 32. In embodiments of the present invention where the substrate 10 is sapphire, the n-type ohmic contact 23 would be provided on n-type GaN layer 12 and/or n-type GaN layer 14.

As described above with reference to Figure 1, buffer layer 11 is preferably n-type AlGaN. Similarly, GaN layer 12 is preferably between about 500 and 4000 nm thick inclusive and is most preferably about 1500 nm thick. GaN layer 12 may be doped with silicon at a level of about  $5 \times 10^{17}$  to  $5 \times 10^{18} \text{ cm}^{-3}$ . GaN layer 14 is preferably between about 10 and 500 Å thick inclusive, and is most preferably about 80 Å thick. GaN layer 14 may be doped with silicon at a level of less than about  $5 \times 10^{19} \text{ cm}^{-3}$ . The superlattice structure 16 may also be provided as described above with reference to Figure 1.

The active region 125 comprises a multi-quantum well structure that includes multiple InGaN quantum well layers 120 separated by barrier layers 118. The barrier layers 118 comprise  $\text{In}_x\text{Ga}_{1-x}\text{N}$  where  $0 \leq x < 1$ . Preferably the indium composition of the barrier layers 118 is less than that of the quantum well layers 120, so that the barrier layers 118 have a higher bandgap than quantum well layers 120. The barrier layers 118 and quantum well layers 120 may be undoped (*i.e.* not intentionally doped with an impurity atom such as silicon or magnesium). However, it may be desirable to dope the barrier layers 118 with Si at a level of less than  $5 \times 10^{19} \text{ cm}^{-3}$ , particularly if ultraviolet emission is desired.

In further embodiments of the present invention, the barrier layers 118 comprise  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$  where  $0 < x < 1$ ,  $0 \leq y < 1$  and  $x + y \leq 1$ . By including aluminum in the crystal of the barrier layers 118, the barrier layers 118 may be lattice-

matched to the quantum well layers 120, thereby providing improved crystalline quality in the quantum well layers 120, which increases the luminescent efficiency of the device.

Referring to **Figure 3**, embodiments of the present invention that provide a multi-quantum well structure of a gallium nitride based device are illustrated. The multi-quantum well structure illustrated in **Figure 3** may provide the active region of the LEDs illustrated in **Figure 1** and/or **Figure 2**. As seen in **Figure 3**, an active region 225 comprises a periodically repeating structure 221 comprising a well support layer 218a having high crystal quality, a quantum well layer 220 and a cap layer 218b that serves as a protective cap layer for the quantum well layer 220. When the structure 221 is grown, the cap layer 218b and the well support layer 218a together form the barrier layer between adjacent quantum wells 220. Preferably, the high quality well support layer 218a is grown at a higher temperature than that used to grow the InGaN quantum well layer 220. In some embodiments of the present invention, the well support layer 218a is grown at a slower growth rate than the cap layer 218b. In other embodiments, lower growth rates may be used during the lower temperature growth process and higher growth rates utilized during the higher temperature growth process. For example, in order to achieve a high quality surface for growing the InGaN quantum well layer 220, the well support layer 218a may be grown at a growth temperature of between about 700 and 900 °C. Then, the temperature of the growth chamber is lowered by from about 0 to about 200 °C to permit growth of the high-quality InGaN quantum well layer 220. Then, while the temperature is kept at the lower InGaN growth temperature, the cap layer 218b is grown. In that manner, a multi-quantum well region comprising high quality InGaN layers may be fabricated.

The active regions 125 and 225 of **Figures 2** and **3** are preferably grown in a nitrogen atmosphere, which may provide increased InGaN crystal quality. The barrier layers 118, the well support layers 218a and/or the cap layers 218b may be between about 50 - 400 Å thick inclusive. The combined thickness of corresponding ones of the well support layers 218a and the cap layers 218b may be from about 50-400 Å thick inclusive. Preferably, the barrier layers 118 the well support layers 218a and/or the cap layers 218b are greater than about 90 Å thick and most preferably are about 225 Å thick. Also, it is preferred that the well support layers 218a be thicker than the

cap layers 218b. Thus, the cap layers 218b are preferably as thin as possible while still reducing the desorption of Indium from or the degradation of the quantum well layers 220. The quantum well layers 120 and 220 may be between about 10 - 50 Å thick inclusive. Preferably, the quantum well layers 120 and 220 are greater than 20  
5 Å thick and most preferably are about 25 Å thick. The thickness and percentage of indium in the quantum well layers 120 and 220 may be varied to produce light having a desired wavelength. Typically, the percentage of indium in quantum well layers 120 and 220 is about 25-30%, however, depending on the desired wavelength, the percentage of indium has been varied from about 5% to about 50%.

10 In preferred embodiments of the present invention, the bandgap of the superlattice structure 16 exceeds the bandgap of the quantum well layers 120. This may be achieved by by adjusting the average percentage of indium in the superlattice 16. The thickness (or period) of the superlattice layers and the average Indium percentage of the layers should be chosen such that the bandgap of the superlattice  
15 structure 16 is greater than the bandgap of the quantum wells 120. By keeping the bandgap of the superlattice 16 higher than the bandgap of the quantum wells 120, unwanted absorption in the device may be minimized and luminescent emission may be maximized. The bandgap of the superlattice structure 16 may be from about 2.95 eV to about 3.35 eV. In a preferred embodiment, the bandgap of the superlattice  
20 structure 16 is about 3.15 eV.

In additional embodiments of the present invention, the LED structure illustrated in Figure 2 includes a spacer layer 17 disposed between the superlattice 16 and the active region 125. The spacer layer 17 preferably comprises undoped GaN. The presence of the optional spacer layer 17 between the doped superlattice 16 and  
25 active region 125 may deter silicon impurities from becoming incorporated into the active region 125. This, in turn, may improve the material quality of the active region 125 that provides more consistent device performance and better uniformity. Similarly, a spacer layer may also be provided in the LED structure illustrated in Figure 1 between the superlattice 16 and the active region 18.

30 Returning to Figure 2, the layer 22 may be provided on the active region 125 and is preferably undoped GaN or AlGaIn between about 0 and 120 Å thick inclusive. The layer 22 is preferably about 35 Å thick. If the layer 22 comprises AlGaIn, the aluminum percentage in such layer is preferably about 10-30% and most preferably about 24%. The level of aluminum in the layer 22 may also be graded in a stepwise

or continuously decreasing fashion. The layer 22 may be grown at a higher temperature than the growth temperatures in the active region 125 in order to improve the crystal quality of the layer 22. Additional layers of undoped GaN or AlGaN may be included in the vicinity of layer 22. For example, the LED illustrated in Figure 2  
5 may include an additional layer of undoped AlGaN about 6-9Å thick between the active regions 125 and the layer 22.

An AlGaN layer 30 doped with a p-type impurity such as magnesium is provided on layer 22. The AlGaN layer 30 may be between about 0 and 300 Å thick inclusive and is preferably about 130 Å thick. A contact layer 32 of p-type GaN is  
10 provided on the layer 30 and is preferably about 1800 Å thick. Ohmic contacts 24 and 25 are provided on the p-GaN contact layer 32 and the substrate 10, respectively. Ohmic contacts 24 and 25 are provided on the p-GaN contact layer 32 and the substrate 10, respectively.

While embodiments of the present invention have been described with  
15 multiple quantum wells, the benefits from the teachings of the present invention may also be achieved in single quantum well structures. Thus, for example, a light emitting diode may be provided with a single occurrence of the structure 221 of Figure 3 as the active region of the device. Thus, while different numbers of quantum wells may be utilized according to embodiments of the present invention, the  
20 number of quantum wells will typically range from 1 to 10 quantum wells.

While embodiments of the present invention have been described with reference to gallium nitride based devices, the teachings and benefits of the present invention may also be provided in other Group III nitrides. Thus, embodiments of the present invention provide Group III nitride based superlattice structures, quantum  
25 well structures and/or Group III nitride based light emitting diodes having superlattices and/or quantum wells.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the  
30 scope of the invention being set forth in the following claims.

**What is Claimed is:**

1. A Group III nitride based light emitting diode, comprising:  
a Group III nitride based superlattice; and  
a Group III nitride based active region on the superlattice comprising at least one quantum well structure comprising:  
a first Group III nitride based barrier layer;  
a Group III nitride based quantum well layer on the first barrier layer;  
and  
a second Group III nitride based barrier layer on the Group III nitride based quantum well layer.
2. The light emitting diode of Claim 1, wherein the at least one quantum well structure comprises from about 2 to about 10 repetitions of the at least one quantum well structure.
3. The light emitting diode of Claim 1, wherein the superlattice comprises:  
a gallium nitride based superlattice having at least two periods of alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$ , where  $0 \leq X < 1$  and  $0 \leq Y < 1$  and  $X$  is not equal to  $Y$ ;  
wherein the first Group III nitride based barrier layer comprises a well support layer comprising a Group III nitride; and  
wherein the second Group III nitride based barrier layer comprises a cap layer comprising a Group III nitride on the quantum well layer.
4. The light emitting diode according to Claim 3, wherein the cap layer has a lower crystal quality than the well support layer.
5. The light emitting diode according to Claim 3, wherein the well support layer comprises a gallium nitride based layer, the quantum well layer comprises an indium gallium nitride layer and the barrier layer comprises a gallium nitride based layer.



6. The light emitting diode according to Claim 3, wherein the well support layer and the cap layer comprises a layer of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  where  $0 \leq x < 1$ .
7. The light emitting diode according to Claim 6, wherein an indium composition of the well support layer and the cap layer is less an indium composition of the quantum well layer.
8. The light emitting diode according to Claim 3, wherein the well support layer and the cap layer comprises a layer of  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$  where  $0 < x < 1$ ,  $0 \leq y < 1$  and  $x + y \leq 1$ .
9. The light emitting diode according to Claim 8, wherein  $x \leq y + .05$ .
10. The light emitting diode according to Claim 3, wherein the well support layer and the cap layer are undoped.
11. The light emitting diode according to Claim 3, wherein the well support layer and the cap layer have a doping level of less than about  $5 \times 10^{19} \text{ cm}^{-3}$ .
12. The light emitting diode according to Claim 3, wherein the cap layer and the well support layer have a higher bandgap than the quantum well layer.
13. The light emitting diode according to Claim 3, wherein a combined thickness of the well support layer and the cap layer is from about 50 to about 400 Å.
14. The light emitting diode according to Claim 3, wherein a thickness of the well support layer is greater than a thickness of the cap layer.
15. The light emitting diode according to Claim 3, wherein the quantum well layer has a thickness of from about 10 to about 50 Å.
16. The light emitting diode according to Claim 3, wherein the quantum well layer has a thickness of about 25 Å.

17. The light emitting diode according to Claim 3, wherein a percentage of indium in the quantum well layer is from about 5% to about 50%.

18. The light emitting diode according to Claim 3, further comprising a Group III nitride based spacer layer between the well support layer and the superlattice.

19. The light emitting diode according to Claim 18, wherein the spacer layer comprises undoped GaN.

20. The light emitting diode according to Claim 3, wherein a bandgap of the at least one quantum well is less than a bandgap of the superlattice.

21. The light emitting diode according to Claim 3, further comprising:  
a second well support layer comprising a Group III nitride on the cap layer;  
a second quantum well layer comprising a Group III nitride on the second well support layer; and  
a second cap layer comprising a Group III nitride on the second quantum well layer.

22. The light emitting diode according to Claim 3, wherein the gallium nitride based superlattice comprises from about 5 to about 50 periods.

23. The light emitting diode according to Claim 3, wherein layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  of the alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  have a combined thickness of less than about 70 Å.

24. The light emitting diode according to Claim 3, wherein  $X = 0$ .

25. The light emitting diode according to Claim 24, wherein InGaN layers of the alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  have a thickness of from about 5

to about 40 Å and GaN layers of the alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  have a thickness of from about 5 to about 100 Å.

26. The light emitting diode according to Claim 24, wherein InGaN layers of the alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  have a thickness of about 15 Å and GaN layers of the alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  have a thickness of from about 30 Å.

27. The light emitting diode according to Claim 3, wherein the gallium nitride based superlattice is doped with an n-type impurity to a level of from about  $1 \times 10^{17} \text{ cm}^{-3}$  to about  $5 \times 10^{19} \text{ cm}^{-3}$ .

28. The light emitting diode according to Claim 27, wherein the doping level of the gallium nitride based superlattice is an actual doping level of layers of the alternating layers.

29. The light emitting diode according to Claim 27, wherein the doping level is an average doping level of layers of the alternating layers.

30. The light emitting diode according to Claim 3, further comprising doped Group III nitride layers adjacent the superlattice and wherein the doped Group III nitride layers are doped with an n-type impurity to provide an average doping of the doped Group III nitride layers and the superlattice of from about  $1 \times 10^{17} \text{ cm}^{-3}$  to about  $5 \times 10^{19} \text{ cm}^{-3}$ .

31. The light emitting diode according to Claim 3, wherein a bandgap of the superlattice is from about 2.95 eV to about 3.35 eV.

32. The light emitting diode according to Claim 3, wherein a bandgap of the superlattice is about 3.15 eV.

33. A Group III nitride based semiconductor device having an active region comprising at least one quantum well structure, the quantum well structure comprising:
- a well support layer comprising a Group III nitride;
  - a quantum well layer comprising a Group III nitride on the well support layer;
  - and
  - a cap layer comprising a Group III nitride on the quantum well layer.
34. The Group III nitride based device according to Claim 33, wherein the cap layer has a lower crystal quality than the well support layer.
35. The Group III nitride based semiconductor device according to Claim 33, wherein the well support layer comprises a gallium nitride based layer, the quantum well layer comprises an indium gallium nitride layer and the barrier layer comprises a gallium nitride based layer.
36. The Group III nitride based semiconductor device according to Claim 35, wherein the well support layer and the cap layer comprises a layer of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  where  $0 \leq x < 1$ .
37. The Group III nitride based semiconductor device according to Claim 36, wherein an indium composition of the well support layer and the cap layer is less an indium composition of the quantum well layer.
38. The Group III nitride based semiconductor device according to Claim 35, wherein the well support layer and the cap layer comprises a layer of  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$  where  $0 < x < 1$ ,  $0 \leq y < 1$  and  $x + y \leq 1$ .
39. The Group III nitride based semiconductor device according to Claim 38, wherein  $x \leq y + 0.05$ .
40. The Group III nitride based semiconductor device according to Claim 35, wherein the well support layer and the cap layer are undoped.

41. The Group III nitride based semiconductor device according to Claim 35, wherein the well support layer and the cap layer have a doping level of less than about  $5 \times 10^{19} \text{ cm}^{-3}$ .

42. The Group III nitride based semiconductor device according to Claim 33, wherein the cap layer and the well support layer have a higher bandgap than the quantum well layer.

43. The Group III nitride based semiconductor device according to Claim 35, wherein a combined thickness of the well support layer and the cap layer is from about 50 to about 400 Å.

44. The Group III nitride based semiconductor device according to Claim 35, wherein a combined thickness of the well support layer and the cap layer is greater than about 90 Å.

45. The Group III nitride based semiconductor device according to Claim 35, wherein a combined thickness of the well support layer and the cap layer is about 225 Å.

46. The Group III nitride based semiconductor device according to Claim 35, wherein a thickness of the well support layer is greater than a thickness of the cap layer.

47. The Group III nitride based semiconductor device according to Claim 35, wherein the quantum well layer has a thickness of from about 10 to about 50 Å.

48. The Group III nitride based semiconductor device according to Claim 35, wherein the quantum well layer has a thickness of about 25 Å.

49. The Group III nitride based semiconductor device according to Claim 35, wherein a percentage of indium in the quantum well layer is from about 5% to about 50%.

50. The Group III nitride based semiconductor device according to Claim 35, further comprising a superlattice and wherein the well support layer is on the superlattice.

51. The Group III nitride based semiconductor device according to Claim 50, wherein a bandgap of the superlattice is from about 2.95 to about 3.35 eV.

52. The Group III nitride based semiconductor device according to Claim 50, wherein a bandgap of the superlattice is about 3.15 eV.

53. The Group III nitride based semiconductor device according to Claim 50, further comprising a Group III nitride based spacer layer between the well support layer and the superlattice.

54. The Group III nitride based semiconductor device according to Claim 53, wherein the spacer layer comprises undoped GaN.

55. The Group III nitride based semiconductor device according to Claim 50, wherein a bandgap of the at least one quantum well is less than a bandgap of the superlattice.

56. The Group III nitride based semiconductor device according to Claim 33, further comprising:

- a second well support layer comprising a Group III nitride on the cap layer;
- a second quantum well layer comprising a Group III nitride on the second well support layer; and
- a second cap layer comprising a Group III nitride on the second quantum well layer.

57. The Group III nitride based semiconductor device according to Claim 33 having from about 2 to about 10 repetitions of the at least one quantum well structures.

58. A Group III nitride based semiconductor device, comprising:  
a gallium nitride based superlattice having at least two periods of alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$ , where  $0 \leq X < 1$  and  $0 \leq Y < 1$  and  $X$  is not equal to  $Y$ .

59. The Group III nitride based semiconductor device according to Claim 58, wherein the gallium nitride based superlattice comprises from about 5 to about 50 periods.

60. The Group III nitride based semiconductor device according to Claim 58, wherein the gallium nitride based superlattice comprises 25 periods.

61. The Group III nitride based semiconductor device according to Claim 58, wherein the gallium nitride based superlattice comprises 10 periods.

62. The Group III nitride based semiconductor device according to Claim 58, wherein layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  of the alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  have a combined thickness of less than about 70 Å.

63. The Group III nitride based semiconductor device according to Claim 58, wherein  $X = 0$ .

64. The Group III nitride based semiconductor device according to Claim 63, wherein InGaN layers of the alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  have a thickness of from about 5 to about 40 Å and GaN layers of the alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  have a thickness of from about 5 to about 100 Å.

65. The Group III nitride based semiconductor device according to Claim 63, wherein InGaN layers of the alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  have a thickness of about 15 Å and GaN layers of the alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$  have a thickness of from about 30 Å.

66. The Group III nitride based semiconductor device according to Claim 58, wherein the gallium nitride based superlattice is doped with an n-type impurity to a level of from about  $1 \times 10^{17} \text{ cm}^{-3}$  to about  $5 \times 10^{19} \text{ cm}^{-3}$ .

67. The Group III nitride based semiconductor device according to Claim 66, wherein the doping level of the gallium nitride based superlattice is an actual doping level of layers of the alternating layers.

68. The Group III nitride based semiconductor device according to Claim 66, wherein the doping level is an average doping level of layers of the alternating layers.

69. The Group III nitride based semiconductor device according to Claim 58, further comprising doped Group III nitride layers adjacent the superlattice and wherein the doped Group III nitride layers are doped with an n-type impurity to provide an average doping of the doped Group III nitride layers and the superlattice of from about  $1 \times 10^{17} \text{ cm}^{-3}$  to about  $5 \times 10^{19} \text{ cm}^{-3}$ .

70. The Group III nitride based semiconductor device according to Claim 58, wherein a bandgap of the superlattice is about 3.15 eV.

71. The Group III nitride based semiconductor device according to Claim 58, wherein a bandgap of the superlattice is from about 2.95 to about 3.15 eV.

72. The Group III nitride based semiconductor device according to Claim 58, wherein the semiconductor device comprises a light emitting diode, the light emitting diode further comprising a Group III nitride based active region on the superlattice.

73. The Group III nitride based semiconductor device according to Claim 72, further comprising a Group III nitride based spacer layer between the active region and the superlattice.

74. The Group III nitride based semiconductor device according to Claim 73, wherein the spacer layer comprises undoped GaN.



75. The Group III nitride based semiconductor device according to Claim 72, wherein the active region comprises at least one quantum well.

76. The Group III nitride based semiconductor device according to Claim 75, wherein a bandgap of the at least one quantum well is less than a bandgap of the superlattice.

77. A gallium nitride based light emitting diode, comprising:  
a gallium nitride based superlattice having at least two periods of alternating layers of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  and  $\text{In}_y\text{Ga}_{1-y}\text{N}$ , where  $0 \leq X < 1$  and  $0 \leq Y < 1$  and  $X$  is not equal to  $Y$ ; and  
a gallium nitride based active region on the gallium nitride based superlattice.

78. The gallium nitride based light emitting diode of Claim 77, wherein a bandgap of the gallium nitride based active region is less than a bandgap of the superlattice.

79. A method of fabricating a Group III nitride based semiconductor device having an active region comprising at least one quantum well structure, comprising:  
forming a well support layer comprising a Group III nitride;  
forming a quantum well layer comprising a Group III nitride on the quantum well support layer; and  
forming a cap layer comprising a Group III nitride on the quantum well layer.

80. The method of Claim 79, wherein the step of forming a well support layer comprising a Group III nitride comprises forming the well support layer at a first temperature;  
wherein the step of forming a quantum well layer comprises forming the quantum well layer at a second temperature which is less than the first temperature;  
and  
wherein the step of forming a cap layer comprises forming the cap layer at a third temperature which is less than the first temperature.

81. The method of Claim 80, wherein the third temperature is substantially the same as the second temperature.

82. The method of Claim 81, wherein the well support layer comprises a gallium nitride based layer, the quantum well layer comprises an indium gallium nitride layer and the cap layer comprises a gallium nitride based layer.

83. The method of Claim 82, wherein the first temperature is from about 700 to about 900 °C.

84. The method of Claim 82, wherein the second temperature is from about 0 to about 200 °C less than the first temperature.

85. The method of Claim 82, wherein the second temperature is less than the first temperature.

86. The method of Claim 82, wherein the indium gallium nitride layer is formed in a nitrogen atmosphere.

87. The method of Claim 82, wherein the steps of forming a well support layer and forming a cap layer comprise forming a cap layer of  $\text{In}_x\text{Ga}_{1-x}\text{N}$ , where  $0 \leq x < 1$  and forming a well support layer of  $\text{In}_x\text{Ga}_{1-x}\text{N}$ , where  $0 \leq x < 1$ .

88. The method of Claim 87, wherein an indium composition of the well support layer and the cap layer is less an indium composition of the quantum well layer.

89. The method of Claim 82, wherein the steps of forming a well support layer and forming a cap layer comprise forming a cap layer of  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ , where  $0 < x < 1$ ,  $0 \leq y < 1$  and  $x + y \leq 1$  and forming a well support layer of  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ , where  $0 < x < 1$ ,  $0 \leq y < 1$  and  $x + y \leq 1$ .

90. The method of Claim 89, wherein  $X \leq Y + 0.05$ .
91. The method of Claim 82, wherein the well support layer and the cap layer are undoped.
92. The method of Claim 82, wherein the well support layer and the cap layer have a doping level of less than about  $5 \times 10^{19} \text{ cm}^{-3}$ .
93. The method of Claim 79, wherein the cap layer and the well support layer have a higher bandgap than the quantum well layer.
94. The method of Claim 82, wherein a combined thickness of the well support layer and the cap layer is from about 50 to about 400 Å.
95. The method of Claim 82, wherein a thickness of the well support layer is greater than a thickness of the cap layer.
96. The method of Claim 82, wherein the quantum well layer has a thickness of from about 10 to about 50 Å.
97. The method of Claim 82, wherein a percentage of indium in the quantum well layer is from about 5% to about 50%.
98. The method of Claim 82, further comprising the step of forming a superlattice, wherein the well support layer is on the superlattice.
99. The method of Claim 98, further comprising the step of forming a Group III nitride based spacer layer between the well support layer and the superlattice.
100. The method of Claim 99, wherein the spacer layer comprises undoped GaN.

101. The method of Claim 98, wherein a bandgap of the quantum well layer is less than a bandgap of the superlattice.

102. The method of Claim 79, further comprising:  
forming a second well support layer comprising a Group III nitride on the cap layer;  
forming a second quantum well layer comprising a Group III nitride on the second well support layer; and  
forming a second cap layer comprising a Group III nitride on the second quantum well layer.

103. The method of Claim 102, wherein the step of forming a second well support layer comprising a Group III nitride comprises forming the second well support layer at substantially the first temperature;

wherein the step of forming a second quantum well layer comprises forming the second quantum well layer at substantially the second temperature which is less than the first temperature; and

wherein the step of forming a second cap layer comprises forming the second cap layer at substantially the third temperature which is less than the first temperature.

104. The method of Claim 103, wherein the third temperature is substantially the same as the second temperature.

105. The method of Claim 80, further comprising forming from about 2 to about 10 repetitions of the at least one quantum well structures.

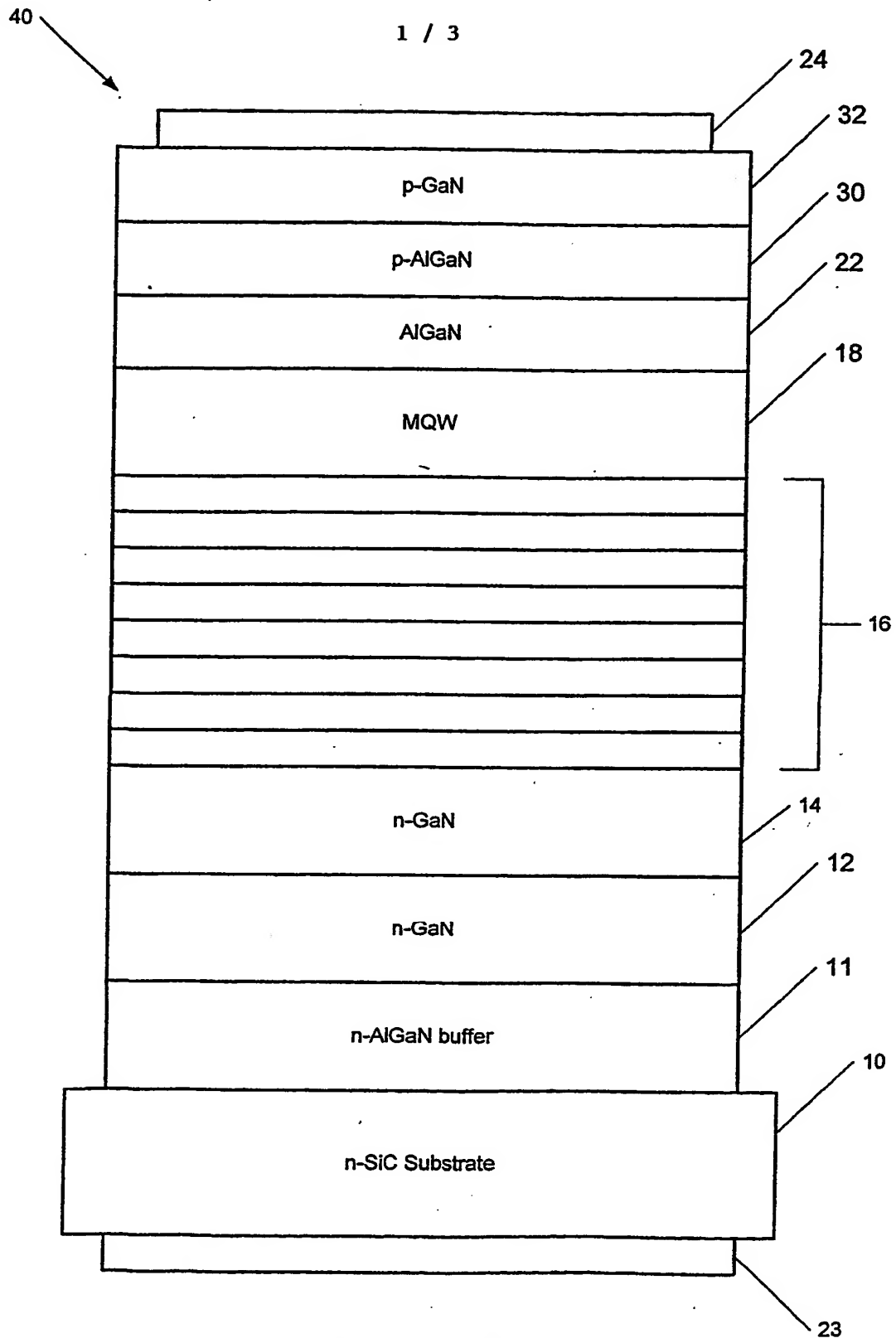


Figure 1

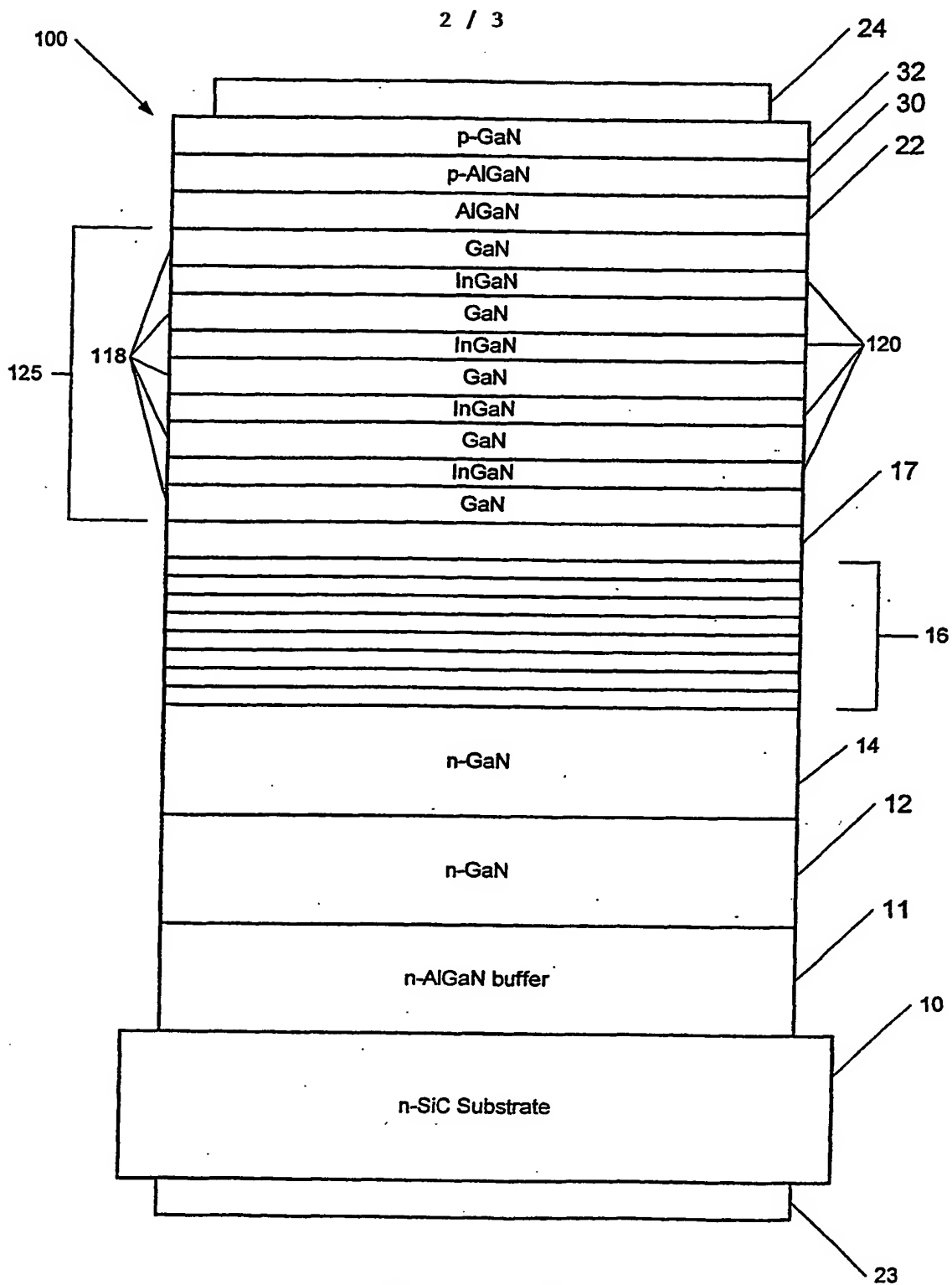


Figure 2

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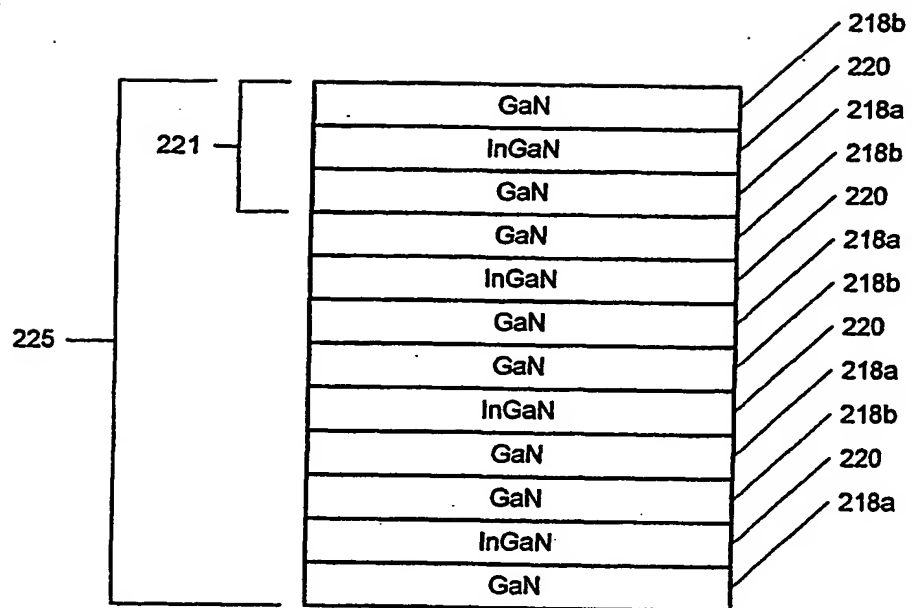


Figure 3